Intel Developer Update is Intel's monthly online news magazine for developers. As the official publication of developer.intel.com, it brings hardware, software, and Web developers the latest information on Intel initiatives, technologies, platforms, and products.

Cover Story

Each month, we run a cover story on the most significant industry announcement, trend, or development for the month.

Featured Articles

Delivering in-depth reports on key platforms, products and technologies, our featured articles provide a monthly source of information on issues affecting developers. Be sure to check in every month for the latest developments driving the evolution of the industry.

Contact the Editor

To make *Intel Developer Update* a better information resource, we invite you to share your thoughts on what we've published or what you'd like to see covered. Comments are always welcome.

Archives

Our archives contain two groups of previously published articles. One group contains all the articles that appeared in *Platform Solutions News*, the earlier version of *Intel Developer Update*. The articles date from September 1997 through August 1999. The other group is set up to contain *Intel Developer Update* articles dating from the inaugural September/October 1999 issue.

Bookmarking

We advise against bookmarking article pages. They're accessible online only during the month the issue is live. Thereafter, they're removed to our archives. Instead, we suggest that you bookmark the PDF (Adobe* Portable Document Format) file versions of the articles. You'll find buttons for the PDF files labeled "print article" in the right navigation section of each article. A PDF for the entire issue is labeled "print magazine" and is located near top right side of the IDU home page.

Table of Contents

(Click on page number to jump to articles)

Note: Intel does not control the content on other company's Web sites or endorse other companies supplying products or services. Any links that take you off of Intel's Web site are provided for your convenience.

Cover Story

Intel® Pentium® 4 Processor: Performance Where Users Need It Most

Christie Rice
Processor Marketing Manager
Intel Desktop Platform Group
Intel Corporation

Overview

State-of-the-art benchmarks (SPEC* CPU2000) confirm that the new Intel® Pentium® 4 processor is the highest performing desktop processor in the world. In SPEC CPU2000 tests, the Pentium 4 processor at 1.50 GHz delivers scores that are 22 percent (integer) to 78 percent (floating-point) faster than the Intel® Pentium® III processor at 1 GHz. The new industry-standard Internet benchmark, WebMark* 2001, which is based on user experiences in connected environments, shows the Pentium 4 processor is 26 percent to 45 percent faster than the Pentium III processor.

While the Pentium 4 processor's great scores may grab the headlines, a big part of the story is that the biggest gains are exactly where developers want them. The Pentium 4 processor delivers performance gains that users can feel in the applications and usages that rule today and tomorrow's desktop.

New Benchmarks for the New Experience

Evolving applications and changing user models make some older benchmarks irrelevant. New metrics must examine how connection speed and the client computer interact to create an overall experience. Your word processing vision may be bounded by how fast you type, and your spreadsheet may never need to calculate any faster, but processor performance is crucial in almost everything else.

WebMark 2001 is an example of the new style of metric. Developed by the respected BAPCo*, marketed by MadOnion.com*, and supported by leading Internet companies, it evaluates user experience in three real-world scenarios: Business to Business (B2B), Business to Consumer (B2C), Business to Employee (B2E or "B") for intranet performance. To ensure that its measurements reflect actual user experiences, WebMark 2001 incorporates relevant and popular Internet technologies into its tests.

Pentium® 4 Processor Benchmarks

The Pentium 4 processor shows its greatest gains in benchmarks that closely approximate real applications and usages. In comparisons with the Pentium III processor 1.0 GHz, WebMark 2001 benchmarks running under Windows* 2000 show these increases for the Pentium 4 processor 1.50 GHz:

- Business to Business (B2B) tests–30 percent faster
- B2C performance–26 percent faster
- B2E or "B" applications–45 percent faster

The WebMark 2001 Overall Score shows a 33 percent improvement over the Pentium III processor.

The high scores given by these metrics are confirmed by tests with actual applications running under Windows* Me (Millennium Edition). Video editing with Ulead VideoStudio* 4.0, for example, speeds up by 40 percent. Video encoding with Microsoft Windows Media Encoder 7.0 is 47 percent faster. MP3 encoding with Canon eJay* MP3 Plus 1.3 is 25 percent faster, saving almost a minute on each CD. Speech recognition with Dragon Naturally Speaking* Preferred 4.0 is 24 percent faster. Gains in 3D benchmarks such as 3D WinBench* 2000 Processor Test and in Gaming such as Quake* III Arena Demo 2 are also dramatic, with improvements of 32 percent and 44 percent.

Future Perfect Computing

System developers face a tough task. They can't design tomorrow's most desired systems by simply repeating the past. The way people use computers changes too fast. Old assumptions can't keep up. Developers have to meet the greatly expanded demands of graphic, video, speech recognition, gaming, and Internet applications. High metrics in the wrong areas won't deliver the experience users want.

These concerns set the challenge for Intel designers–how to develop a new processor family that would meet and surpass those demands today and in the future. The next generation of processors had to anticipate the next generation of computing.

The Intel Advantage

The desire to stay well ahead of the curve sparked the development of Intel® NetBurst™ micro-architecture. Its design innovations will drive performance leadership for years to come. These advantages are fully incorporated in the Pentium 4 processor.

Hyper-pipelined Technology gives the Pentium 4 processor significantly higher performance, frequency, and headroom. The Rapid Execution Engine enables key instructions to run at twice the core frequency. The 400-MHz System Bus provides the Pentium 4 processor with a 3.2-GB/second data transfer rate–three times the bandwidth of the Pentium III processor. The Execution Trace Cache stores decoded instructions to reduce latency and make full use of the Pentium 4 processor's speed. The architecture's Streaming SIMD Extensions 2 expand Intel's MMX™ technology with 144 new instructions that accelerate video, multimedia, 3D, imaging, and encryption operations.

Another Intel advantage that enhances Pentium 4 processor performance is the new Intel® 850 chipset. Carefully optimized for the 400-MHz system bus, the 850 chipset balances performance with dual RDRAM channels.

Power for the New Visual Internet

The convergence of Web access with processor-intensive display technologies is creating a new "visual" Internet. Applications that depend on client performance, such as Macromedia Flash* and RealPlayer* have changed the way we experience the Internet. Web site designers know that animation, 3D graphics, and video greatly increase traffic. Expectations for complex imaging, streaming video, speech, 3D, and multimedia applications have become the rule–not the exception.

As bandwidth limitations fade away with fatter pipes and better compression, common Web graphics and animations leave older PCs and processor designs gasping for breath. Content-rich commercial sites require high-performance PCs to create the experience regardless of the connection speed. New usage models like B2B, B2C, and B2E Intranet demand multitasking PCs that can keep up with the appetites for Web-delivered information, training, and multimedia products. The success of the new Internet will depend on superior systems built around superior processors. The Pentium 4 processor fits the bill here.

Summary

The Intel Pentium 4 processor delivers the world-class performance you expect. It is the highest performing desktop processor in the world as measured by SPEC CPU2000. The Intel Pentium 4 processor delivers its performance gains where PC designers need them most–in the real-world processor-intensive applications that dominate today and tomorrow's desktop experience. This Intel advantage is confirmed by performance on real applications as well. The Pentium 4 processor will set the standard for years to come.

More Info

For more information on the Intel Pentium 4 processor, visit the Intel Pentium 4 processor section of the Intel Web site.

The Intel Pentium 4 processor presentation (PDF, 537K) delivered at the Intel Developer Forum Conference, Spring 2000, is available from the Intel Pentium 4 processor section of the Intel Web site as is the presentation from the Fall 2000 Conference (PDF, 811K).

For an overview of the Pentium 4 processor and its Intel NetBurst micro-architecture, see "Introducing the Intel® Pentium® 4 Processor" by Christie Rice in the November 2000 *Intel Developer Update.*

For additional information on Pentium 4 processor performance, visit the Intel® Processor Performance site.

Author Bio

Christie Rice is the processor marketing manager for Intel's Desktop Platform Group. During her four years with Intel, Christie has been part of the marketing team for both the Intel Pentium III processor and the new Intel Pentium 4 processor.

Christie began her Intel career with the Flash memory group, where she earned industry recognition for enabling the industry to store code and data in Flash components. Prior to joining Intel, she worked for 14 years in circuit board and system design and marketing.

A graduate of New Mexico State University, Christie has a B.S. in electrical engineering. She also has an M.S. in electrical engineering from Southern Methodist University and an M.B.A. from the University of Dallas.

Column

From the Editor
Donna Loveland
Managing Editor
Intel Developer Update Magazine
Intel Corporation

Column

Last month's cover story gave you a first look at the new Intel® Pentium® 4 processor, taking you on a tour of its NetBurst™ micro-architecture. Many of you wrote back asking about performance. We have the answer in this month's cover story. The Pentium 4 processor is *fast*–and we've got the numbers to show you. We also have details about a new Pentium 4 processor-based board.

In addition, we have not one but *two* articles about the Instantly Available PC (IAPC) technology that just won the U.S. Environmental Protection Agency's 2000 Climate Protection Award. We're following up August's popular "Zero to OS in 2.2 Seconds" with another great piece on rapid boot technology *plus* an article on open course boot integrity services (BIS). We also have the latest on Voice over IP, XML for e-Business, and the new Intel® Integrated RAID Controller GSU31 for networked servers.

Here's a summary.

Intel® Pentium® 4 Processor: Performance Where Users Need It Most–*cover story*– State-of-the-art benchmarks (SPEC* CPU2000) confirm that the new Intel Pentium 4 processor is the highest performing desktop processor in the world. The biggest gains are exactly where developers want them–in the applications that rule today and tomorrow's desktop.

The Intel® Desktop Board D850GB–The new Desktop Board D850GB is Intel's highest performance desktop board, providing the power needed to enhance video and 3D applications as well as Internet experiences. It also provides the scalability to support bandwidth-intensive applications in the future.

PCI-D3 Tests for Instantly Available PCs–IAPC add-in devices must be tested singly and as part of an IAPC-capable system to verify power-management functionality. Intel offers PCI-D3 tests that give developers a valuable way of verifying IAPC-capable PCI graphics, audio, modem, and network devices.

Testing Instantly Available PCs to Ensure a Robust Product–OEMs are shipping IAPC products now, and developers must test hardware and software power management features. Intel's test matrix delivers a high-level methodology for IAPC-compliance tests. The procedures were optimized through work with OEMs, IHVs, and ISVs.

Building a Fast Boot System–with Intel® Rapid BIOS Boot–The computer industry as a whole is calling for reductions in boot times. Intel is taking a leading role in related industry-wide initiatives by developing Rapid BIOS Boot (RBB). This article explains how to take full advantage of RBB and outlines key steps for reducing boot times.

Intel Releases BIS Server Components as Open Source–The Boot Integrity Services (BIS) API represents an important step in helping safeguard PC integrity during preboot management for network PCs. Intel is releasing the BIS server component as open source software that can be deployed royalty-free to enhance the security of PXE- based preboot operations.

Intel® Architecture in the Voice over IP Gateway–The convergence of voice and data is increasing the value and usefulness of the Internet. The promise of transporting traditional telephony services over IP- (Internet Protocol) based networks is leading to the development of cost-effective gateway equipment based on embedded systems.

Intel® XML-based Solutions for e-Business Data Centers–XML (eXtensible Markup Language) is emerging as the cross-platform data format standard for e-Business. Developers are now creating XML-based applications, and Intel is helping drive XML adoption with a family of XML networking appliances.
Intel® Integrated RAID Controller GSU31–As the Internet becomes pervasive, organizations of all sizes are becoming dependent on mission-critical information stored on Intel® Architecture-based networked servers. This new small form-factor controller lets server OEMs offer customers a choice of affordable RAID options.

Be sure to use the links in the “More Info” section of each article to get details on these significant topics.

Enjoy.

Author Bio

Donna Loveland is the editor of *Intel Developer Update* magazine. She joined Intel's Platform Marketing group in 1999 as the editor of Platform Solutions News. Donna began her career with Intel in 1982 as a technical editor in an advanced microprocessor development group. Since then, she's held technical and marketing positions in leading-edge technology areas ranging from stereoscopic display to digital broadcast to scalable online content. Donna has a B.A. degree in English from the University of Rochester and an M.A. in Expository Writing from the University of Iowa.

Departments

Desktop

Building a Fast Boot System–with Intel® Rapid BIOS Boot

Justin Whitney
Senior Product Marketing Engineer
Intel Architecture Marketing Group
Intel Corporation

Dan Ragland
Technical Marketing Engineer
Intel Architecture Marketing Group
Intel Corporation

Overview

Are you tired of waiting for your PC to boot? Well, you're not alone. For most computer users, a lengthy boot time is not only frustrating, it also creates a perception of poor system performance. For OEMs, systems with slow boot times generate more tangible problems by creating bottlenecks in the manufacturing process, increasing costs, and reducing productivity.

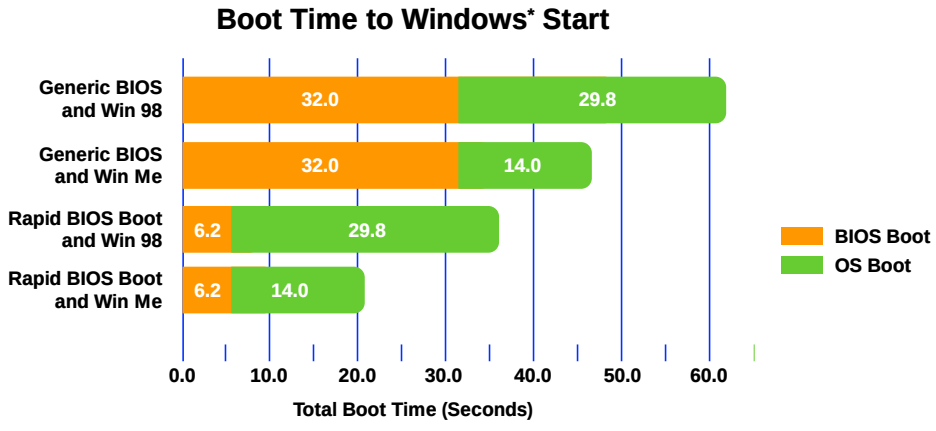
As a result, the computer industry as a whole is calling for reductions in boot times. Intel is taking a leading role in related industry-wide initiatives and has developed Rapid BIOS Boot (RBB) to enable quicker system boots. This article explains how to take full advantage of RBB and outlines several other key steps for reducing boot times.

Three Areas for Improvement

Three major factors affect overall PC boot time–the BIOS boot process, hardware selection and configuration, and choice of OS and software settings. Making well-informed choices in each of these areas significantly reduces boot times.

BIOS Optimization

Typically, a large portion of the boot interval is used by the BIOS (shown in Figure 1) as it initializes I/O devices, performs power-on self test (POST), and scans system buses and main memory.



In this test, Intel® Rapid BIOS Boot resulted in an 80 percent reduction in POST time and a 56 percent reduction in the time to Windows Millennium Edition launch

Figure 1

Intel® Rapid BIOS Boot has streamlined this process, cutting POST time from about 30 seconds to approximately 7 seconds, which reduces overall system boot time by approximately 50 percent. This time reduction was achieved through BIOS code optimization, not trade-offs in functionality.

You can enhance these time savings further with the following BIOS configuration choices. Key steps are highlighted with a §.

- § *Enable Intel Rapid BIOS Boot*. This important step saves 10 to 12 seconds by eliminating the memory scan and floppy seek, which are typically unnecessary.
- *The primary hard drive should be selected as the first boot device in the Boot Order Configuration*. If you choose another device, a CD-ROM drive, for example, the boot process will require several extra seconds to determine whether the installed media is bootable.
- *IF YOU'RE NOT USING IT, TURN IT OFF*. As you disable each of the following functions, you save small increments of time, which quickly add up.
  - Disable USB legacy support on systems not using a USB keyboard or mouse.
  - Disable unused IDE channels.
  - Disable the floppy disk controller if there's no floppy drive.
  - Enable only event logging on systems that require the feature.
  - § Disable LAN when networking is not required–this saves 6 to 8 seconds.
  - Disable unused I/O ports (parallel and serial).

Hardware Selection and Configuration

Hard drive spin-up, graphic card initialization, and other hardware start-up functions all require precious boot time. Here are some timesaving guidelines for hardware purchase and configuration. Key areas are highlighted with a §.

- § *Hard drive selection.* Choosing the right hard drive can reduce boot time by 4 to 8 seconds. The key is to select a hard drive with a faster spin-up time–often referred to on datasheets as "power-up to data-ready." In general, look for spin-up times of less than 8 seconds. You may also need to evaluate "power-up to data-ready" times in relation to data transfer rates. For example, 7,200 RPM drives tend to spin up slower than 5,400 RPM drives, but their data transfer rates are better and can therefore load the operating system much faster.
- *ATAPI device selection.* Avoid devices, such as CD-ROM drives and removable storage drives, that are slow to initialize during POST.
- *Add-in Cards.* The BIOS cannot control the amount of initialization time used by option ROMs of third-party add-in cards. As a result, you need to consider whether the specific capabilities provided by add-in cards are worth the extra seconds they add to the boot process. Request faster loading option ROMs from your hardware vendors.
- § Video cards may increase boot time by 6 to 8 seconds. So avoid cards with slow-loading option ROMs, such as animated manufacturer logos.
- If your system requires a SCSI controller, avoid cards with slow device detection, and be sure to properly configure your SCSI devices. Use the SCSI controller's BIOS to disable the CD-BOOT if it's not needed.

OS Optimization

Your choice of operating system and applications plays a big role in boot times. Key items are highlighted with a §.

Operating system choices: Microsoft has optimized Windows* Millennium Edition for boot performance. While Windows 98 takes approximately 30 seconds to boot, the Millennium Edition requires only 10 to15 seconds–a reduction of at least 50 percent.

For even better boot times, consider using a Linux* operating system.
§ *Optimize further.* After you install Windows Millennium Edition, run the "Defrag" program, which contains the Intel® Application Launch Accelerator. This step, in some configurations, may shave an additional 2 to 4 seconds from boot time by optimizing file location on the hard drive.

§ *Install the correct drivers.* Additional time savings have been observed in conjunction with the installation of Intel® Ultra ATA Storage Drivers. The increased hard drive data transfer rates may reduce OS load times by as much as 14 percent.

§ *Other software choices.* Watch out for applications that slow down boot time, particularly programs that are loaded into the system tray or start-up folder, or others that load upon OS boot. These programs typically include hot sync managers, program schedulers, sound utilities, and graphics applications. By removing unnecessary applications from the start-up sequence, you can save anywhere from 2 seconds to 20 seconds.

Testing Your Changes

Here's how to test your changes and see what effect they have on boot time.

- *Set a benchmark.* Begin by measuring your initial boot time, before changing BIOS settings or hardware configurations.
- *Measure "power on" to active desktop.* Start timing by simultaneously pressing the start button on your stopwatch and the power button on your PC. The moment the hourglass on the desktop turns into a pointer, press the stop button on your stopwatch. This is your total system boot time.

Tests were performed on systems with a 733 MHz Intel® Pentium® III processor, 128 MB of SDRAM, D815EEA Intel Desktop Board with integrated graphics, and Western Digital AA and BA series hard drives operating at 5,400 and 7,200 RPM.

Boot times may vary with system configuration. (Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel® products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.)

Summary

Improved boot times benefit end users and manufacturers alike.

- *For end users* faster start-up times improve the perception of PC performance and increase user satisfaction. Today, many users "save up" projects for a single PC session, just to avoid the frustration of long boot times. As boot times decrease, the frequency of PC usage increases.
- *For OEMs/Integrators* shorter boot times improve manufacturing "beat rates," reduce burn-in time, and enhance overall productivity.

Encourage hardware and software vendors to respond to the computer industry's request for faster boot times. That means communicating your need for faster loading operating systems and application software, as well as faster initializing hard drives, graphics cards, and other devices.

By following the steps outlined in this article, you can reduce frustration for PC users, increase customer satisfaction, and support manufacturing efficiencies.

More Info

The IDU article titled "Zero to OS in 20.2 Seconds," from the August 2000 issue, provides more background information on the Intel Rapid BIOS Boot. It includes test results for optimized systems and provides recommendations for upgrading an older BIOS to Rapid BIOS Boot.

For additional technical details that can help you reduce boot times, visit the PC Design Guides site as well as the Web sites for specific hard drive OEMs and graphics card vendors.

Author Bio

Justin Whitney is a senior product marketing engineer within the Intel Architecture Marketing Group. His project responsibilities have included Intel Rapid BIOS Boot, Intel® Express BIOS Update, and the Superconducting Liquid Cryogenic Level Sensor, for which he holds a patent. Justin holds a B.S. in mechanical engineering from Northwestern University.

Dan Ragland is a technical marketing engineer within the Intel Architecture Marketing Group. He is responsible for supporting the technical aspects of new Desktop Board products and technologies.

The Intel® Desktop Board D850GB

Bob Fried
Product Marketing Engineer
DPB-Boards and Systems Marketing
Intel Corporation

Overview

It's a well-known fact that Internet usage has skyrocketed. According to Strategy Analytics, a market research firm based in Wellesley, Massachusetts, 91 percent of U.S. households will be online, and the average online home will have 2.7 Internet-connected devices by 2005. As usage has grown, so too have the bandwidth requirements for each user. Bandwidth-intensive Internet applications such as streaming video have become increasingly popular, as have broadband interactive voice, video, and games. Internet usage is currently 350 petabytes per month, with streaming media already accounting for more than 10 percent of this total, according to RHK, a leading industry market research firm specializing in the telecommunications market, based in South San Francisco, California.

Handling these applications requires powerful and high-performing desktop systems. The Intel® Desktop Board D850GB meets these requirements by offering the highest performance available in a desktop platform. The board is the first Intel® product to incorporate the latest Intel® Pentium® 4 Processor and the new Intel® 850 chipset, which supports dual RDRAM channels and the Intel® Pentium® NetBurst™ micro-architecture.

Performance Enhancements

The Intel Desktop Board D850GB is available as a boxed solution through normal Intel desktop board distribution channels. OEMs integrating the board into their desktop PC and low-end workstation systems will gain performance boosts through the following capabilities:

- *Support for Intel 850 chipset*. This is the latest Intel® chipset to support the new Pentium 4 Processor enhanced features including the NetBurst micro-architecture with dual RDRAM* channels, which provides a 3.2-GB per second memory bus bandwidth to match the Pentium 4 Processor's system bus requirements.
- *System bus speeds of 400 MHz* enable performance improvements in the high-bandwidth and concurrent applications required for today's emerging Web technologies.
- *Intel® Rapid BIOS Boot* speeds up the Power on Self Test (POST) for faster system availability.
- *Four RDRAM RIMM sockets* support the fastest available memory types, PC800 and PC600 RDRAM memory from 128 MB to 2 GB.
- *USB support*. The D850GB desktop board features optional support for USB 2.0 technology (SKU targeted availability in Q2 '01), which increases USB bandwidth by up to 40 times.
- *Communications and Networking Riser* (CNR) for audio, modem, LAN, and HPNA support.
- *Ultra ATA/100 disk support.*
- *Five PCI slots.*
- *AGP 4X 1.5 V.*
- *Instantly available PC* (Suspend-to-RAM).

Benefits

The Desktop Board D850GB is the first Intel product to support both the new Pentium 4 chip and the 850 chipset, which means that the board offers all the design strengths of the next-generation Intel products in a single product. As a result, it is able to provide the headroom today's consumers need to meet current requirements for Internet bandwidth, and it will also support Intel's new direction for some time in the future.

Intel's rigorous design and testing requirements makes this one of the highest quality and most reliable products available today.

Summary

The Desktop Board D850GB is Intel's highest performance desktop board, providing the power users need to enhance their video and 3D applications as well as their Internet experiences, from simple Web surfing to video-on-demand. The product will also provide the scalability users need to support bandwidth intensive applications in the future.

More Info

More information on this product is available on Intel's Developer site.

Author Bio

Bob Fried is a product marketing engineer in the Performance and Value Product Marketing Group in DBSM. Bob joined Intel in 1999 and was involved in the launch of the D820LP and D850GB products. Prior to joining Intel, Bob worked as a manufacturing engineer in the high-tech industry for five years. Bob received his B.S. in industrial and management engineering from Montana State University and his M.B.A. from Portland State University.

Testing Instantly Available PCs to Ensure a Robust Product

Jerzy Kolinski
Systems Architect
Intel's Architecture Lab
Intel Corporation

Overview

Personal computers with Instantly Available PC (IAPC) technology deliver great benefits to users by eliminating lengthy boot times. IAPCs also deliver substantial benefits by saving energy when the system is in the idle state and still maintaining communication capabilities. IAPC power-management features must be implemented in both hardware and software to ensure reliable and robust system behavior. Because a complete, integrated system includes add-in cards, external peripherals, the operating system, and applications, the entire system must be tested to verify that the power management functions work properly on the system level. It takes only one malfunctioning or noncompliant IAPC peripheral device or driver to cause system misbehaviors during suspend and resume cycles.

Original equipment manufacturers (OEMs) are shipping IAPC products today. This means that developers must include and test power management features now for hardware components such as motherboards, peripheral component interconnect (PCI) add-in cards, and external peripheral devices. And software developers need to design and test operating systems, applications, and drivers that have power-management features.

Intel's test matrix gives you a high-level methodology for IAPC-compliance tests. We developed these test procedures by working with OEMs, Independent Hardware Vendors (IHVs), and Independent Software Vendors (ISVs). Their feedback, comments, and the cooperative effort as a whole has allowed us to determine a method for testing IAPC compatible systems. Passing the Intel® IAPC tests helps you test for stability and robustness.

Intel recommends that you perform IAPC compliance tests in three important categories: motherboard tests, peripheral tests, and system-stress tests.

Motherboard Tests

Motherboard tests verify that the motherboard implements basic IAPC functions. The test configuration here is limited to the motherboard, graphics device, hard drive, and power supply. The basic system functions tested are those that allow the system to properly enter and resume from the S1, S3, and S4 sleep states. These tests also examine power dissipation in the sleep state, system resume times from various sleep states, and the quality of the power delivery subsystem.

The motherboard tests include:

- System BIOS test to ensure that the BIOS is ACPI-compliant.
- System power measurement to verify that the system consumes less than 5 watts in the S3 sleep state.
- Resume time measurement (should be less than 10 seconds). Resume time depends on the system BIOS, OS, device drivers, and the hard drive spin-up time.
- Dual-mode power delivery tests, which ensure that the memory, PCI, and USB (universal serial bus) voltages remain within regulation through the suspend/resume transitions.
- Real-time clock (RC) wake capabilities, in which the system is put to sleep and awakened after a specified time.

The resume time measurement can uncover issues with the BIOS, such as the BIOS waiting for the hard drive to spin up before BIOS releases control to the operating system. We recommend that IAPC designs use hard drives with fast spin-up times, and that developers remove hard drive wait loops.

However, the most common problems in motherboards are in the power delivery subsystems. The power delivery subsystem must provide sufficient power in the S3 state for PCI, USB, and PS/2 wake-capable devices.

Common problems seen in motherboards include:

- *Inappropriate FETs or lack of FETs.* While testing numerous systems, we found that in many systems, PCI Vaux voltage and USB voltage in S3 states were below minimum specified thresholds. Some motherboards do not use field-effect transistor (FET) at all to switch between 3.3V standby (S3) voltage and 3.3V main (working-state S0) voltage. Instead, these systems route 3.3V standby voltage directly or by using jumper switches to PCI 3.3 Vaux pins. In these cases, the designs do not provide sufficient power for all types of PCI add-in cards according to PCI specifications. In cases where the voltage is out of regulation, the reliability of the system is compromised.
- *Lack of Sufficient Standby Current.* In some systems, we found that the power delivery subsystem does not provide sufficient standby current to support wake-capable devices such as PCI, USB, and PS/2 devices. The minimum requirement for an IAPC system is to use a power supply with 720 mA of standby current. However, developers should use power supplies with more than 720 mA standby current to support systems with multiple PCI, USB, and PS/2 wake-capable devices. Standby current provided by the power supply must be calculated based on the maximum configuration of wake-capable devices supported by the system.

After verifying the motherboard through these tests, you should have confidence that the motherboard is working properly. You should also be confident that the motherboard supports the power-management features required for integrating the complete IAPC-capable system.

Peripheral Tests

Peripheral devices are tested after the motherboard is verified for IAPC functionality. Peripheral devices include PCI add-in cards, USB devices, hard drives, and CD-ROM devices. The peripheral-device tests verify that devices work properly after a suspend/resume sequence. These tests also verify wake-support of wake-capable modem, LAN, and communications network riser (CNR) devices.

We recommend suspend/resume testing of the following subsystems and peripherals:

- Graphics and audio.
- Modem/LAN and CNR–functionality and wake capabilities.
- USB devices–wake capabilities for devices such as keyboards, mouse, and modems.
- Hard drives, CD-ROMs, and DVD–ensure that multiple configurations work properly after resume.
- Parallel and serial devices.
- PS/2 mice and keyboards–functionality and wake capabilities.

Issues with Peripheral Devices

The main purpose of peripheral testing is to make sure that the hardware devices and drivers properly support power-management. For example, the state of the system upon resume must be exactly the same as before the sleep request. It is also important to support power-management broadcast messages that are sent by the operating system before the system enters the S3 state. If the device driver does not support power-management messages, the system may malfunction during resume.

Peripherals should be tested both individually and in different system configurations. This is critical because power-management issues for that device may not become apparent until the device is tested in a fully integrated system.

Some common problems seen with peripheral devices:

- *Failures upon Returning from S3 Standby.* The most common problems seen with peripherals is a lack of power-management features in the device driver. For example, after installing a peripheral device, the system may not enter S3, or it may stop responding upon resume. However, the system suspends and resumes correctly when the device and driver are uninstalled or removed. This indicates that the problem is likely to be the peripheral device, not the system.
- *Rejecting the Standby Request.* Some devices and applications reject the system's request to enter S3 because they do not properly implement power-management features. We observed this problem with network cards, SCSI cards, DVD players, and USB storage devices.
- *IDE Storage Devices.* Some systems resume properly with one hard drive and CD-ROM, but fail with multiple hard drives and CD-ROM configurations. This usually happens upon resume because of insufficient initialization routines in BIOS.

It is critical that the drivers and peripherals are tested both individually and within the system, since a single malfunctioning driver can affect overall system behavior.

Device Responses

Here are some recommended optimum responses for peripheral devices that will help developers enable the full benefits of an IAPC system:

- *Keyboards, mice:* Upon resume, these devices should work exactly as they did before the sleep state.
- *Printers, scanners:* The system should not go to sleep until the printer or scanner is idle. For example, the system should not go to sleep until the printer is done printing all files in the queue.
- *Hard drives:* Performance must be the same upon resume as it was before the system entered S3 state.
- *Graphics:* Should return to the same screen that was previously displayed. For example, a moving object such as a bouncing ball should be displayed upon resume exactly where it had previously been when the system went to sleep. For some graphics-intensive applications, we recommend that the application be paused before the system can enter standby and that, upon resume, the user is prompted to restart the application.
- *Audio:* The system either continues playing audio files, or it pauses the application and asks the user whether it should resume playing the previously open file.
- *DVD:* The application should be paused before the system enters the standby state. Upon resume, users should be prompted as to how to proceed. For example, users should be asked if they want to start playing again exactly where they left off, rewind the movie 60 or 120 seconds before the movie restarts, or halt/quit the previously running movie file. The picture quality, when it resumes, should not be jerky or skip frames due to system initialization problems.
- *Cameras:* Video-streaming should resume from the same point at which it was paused while going to S3.
- *Network communications:* If connected via LAN, the system should maintain the network connection while in S3. After resuming, the system functionality should be exactly the same as before entering the sleep state. The system should also wake when other users are accessing data on the shared drive.

System Stability Tests

The last set of tests are system stability tests. The system stability tests ensure that the system is stable and robust and functions properly over an extended period of time. Stability tests uncover marginal power delivery designs, system-timing issues, and driver and/or application memory leaks.

The system stability tests use three different wake mechanisms:

- *Real-time clock*–the Suspender test
- *Power button*–via a manual test or an automatic switch connected to the power button
- *PCI/PME signal*–the waker/dozer test

We have found that running the Suspender application for 1,000–2,000 cycles in a complete system configuration is sufficient to detect most problems. Running 1,000–2,000 cycles gives you confidence that the system configuration (including hardware and drivers) is robust. A 1,000 cycles is equivalent to suspending/resuming the system five times a day for six months without rebooting.

After successfully running the Suspender test 1,000 times, the power button test and waker/dozer test may be run only 10–100 times to ensure that the power button and PCI power-management event (PME) interface is working properly.

Both the Suspender test and waker/dozer tests have been developed by Microsoft, and are included in the HCT test suite, which is available from Microsoft.

Summary

All desktop systems shipped in 2001 will be required to implement IAPC technology. Intel's IAPC test matrix provides high-level methodology for testing motherboards.

The motherboard tests examine the power delivery subsystem, measure resume time, and measure sleep-state power. Peripheral tests verify that each device and its corresponding driver is IAPC-compliant and functions properly after the suspend/resume sequence. The system-stress tests make sure that complete system (including add-in cards, peripheral devices, and applications) is robust and functions properly over many cycles.

These tests were developed in a cooperative effort with OEMs, IHVs, and ISVs, and provide a method for testing devices and systems for IAPC compliance. We recommend that you run these tests for all IAPC-capable motherboards, peripheral devices, and systems.

More Info

A white paper titled “Testing Instantly Available PC” is available at the Intel’s Developer Update site. Information about specific tests recommended by the IAPC test matrix can be found in the IDU article titled “PCI-D3 Tests for Instantly Available PCs.”

Specific tools for testing motherboards, peripherals, and drivers are available in the Microsoft HCT test suite, and through Intel’s test-related papers and articles on the Intel’s Developer Update site. The IAPC Web page provides additional information about IAPC technology and IAPC-compliant motherboards, peripherals, and drivers.

IAPC Technology Wins EPA 2000 Climate Protection Award
With its Annual Climate Protection Awards, the United States Environmental Protection Agency (EPA) honors the extraordinary accomplishments of individuals, companies, and organizations that have made significant contributions to protecting the environment. Intel’s Instantly Available PC Technology was chosen along with nine others to receive this award in Washington, D.C. on October 31, 2000.

Author Bio

Jerzy Kolinski joined Intel in 1989, and is a systems architect at Intel’s Architecture Lab. He is a member of the Intel corporate task force responsible for developing new architecture to enable standardized desktop power-management with reduced resume latency. Prior to his involvement in power-management architecture, Jerzy led design teams in developing high-performance desktop systems and multiprocessor server systems. He earned his B.S.E.E. from the University of Illinois, and his M.S.E.E. from Portland State University.

PCI-D3 Tests for Instantly Available PCs

Ram Chary
Software Systems Architect
Intel's Architecture Lab
Intel Corporation

Overview

With the emergence of advanced configuration power interface (ACPI) and other power-management technologies (including PCI Power Management, OnNow™ and InstantlyAvailable™), it is important for all components of a PC system to participate in system-wide power management.

System-wide power management can be achieved only if developers of add-in devices design those devices to be power managed and if they test and verify their devices within systems that support the various power-management features. Intel offers Instantly Available PC (IAPC) tools and test suites for testing IAPC-compatible PCI devices. These tests help developers build devices and drivers capable of participating in the new power-management architecture.

About the Tests

The PCI-D3 tests verify the sleep state (D3) functionality for devices in IAPC systems that are going to the S3 (system) sleep state. There are two main types of tests in the IAPC PCI-D3 device test suite: switch tests and staging tests. A switch test requires that the PC be put into S3 manually, using the power button. The switch test also wakes the PC manually via the power button. A staging test uses Microsoft Windows* power-management options to set up the PC for the standby state. This test specifies, for example, that the system will enter S3 after a certain interval of inactivity, such as two or three minutes.

Remember that a peripheral device can go into the D3 state even if the system is still in the S0 state. Although the system may be active (S0), the device itself may have been inactive and programmed by the operating system to go to the D3 state. For example, a modem may go to D3 when not in use, even though the system itself is still active.

All tests must be run on systems that are validated IAPC implementations. The only variable in each test should be the candidate peripheral device. This means that each IAPC-capable peripheral device in the system must correctly support D3. Except for the candidate device, each IAPC-capable device must be a known-good device and must work well in a system that supports S3. Intel's site for the Reference Platform Program includes lists of known-good devices and systems.

Some tests require that you install additional software on the systems, including Microsoft DirectX* 7.0 SDK and the Microsoft Combat Flight Simulator application.

PCI-D3 Graphics Device Tests

These tests examine PCI and AGP graphics devices and drivers for correct power-management behavior in S3 systems. These tests verify that the graphics hardware and driver:

- Successfully allow the system to enter the S3 sleep state
- Successfully allow the system to wake from the S3 sleep state
- Are fully functional on resume from the S3 sleep state

The graphics device tests consist of four main procedures:

1. Suspend/resume switch tests (S3 state).
2. Suspend/resume staging test (S3 state).
3. Reference application switch test (S3 state), which uses Microsoft Combat Flight Simulator.
4. Suspend/resume using a collection of DirectDraw* and D3D (Direct 3-Dimensional) samples from the DirectX 7.0 SDK. This is an automated test that runs a series of DirectX and D3D samples and programmatically cycles the system to the S3 state while the samples are running. The device under test passes if, on resume, no video artifacts are seen on the sample that is running.

PCI-D3 Modem Tests

There are two types of PCI-D3 modem tests: tests that validate correct basic behavior and wake-on-ring tests (described later). The basic PCI-D3 Modem test verifies that the modem hardware and driver successfully allows the system to go to S3 and resume. The modem D3 test verifies that, when a modem and its corresponding drivers are installed, the target system can still correctly enter and resume from S3.

There are two main procedures in the modem D3 functionality test:

1. Suspend/resume switch test (S3 state).
2. Suspend/resume staging test (S3 state).

PCI-D3 Modem WOR Test

The wake-on-ring (WOR) test is a functionality test for the modem. This test requires two connected systems: the target system (which has the candidate modem) and a server system (which need not be an IAPC-capable system).

The WOR capability tests verify that:

- When the target system is in S3 and it receives an incoming call to wake, the modem responds to the incoming ring and wakes up the system successfully.
- The target system's modem is fully functional after the system resumes from S3 due to a WOR event. The server and target systems exchange a known-good file and ensure (after the system resumes from S3) that no data corruption occurs during the send/receive process.

Waker/Dozer Test

Intel has added the waker/dozer HCT test to the PCI-D3 Modem functionality tests. This test also verifies D3 support in PCI modems and requires two systems: a dozer and a waker. One system dozes (S3), while the other system (waker) creates the event that tells the dozer to resume from S3.

In earlier versions of HCT, the waker/dozer test takes the system to the S1 sleep state when entering standby. In the latest HCT, the dozer does go to the S3 state (if the system supports the S3 sleep state).

PCI-D3 Network Test

As with modems, there are two main PCI-D3 Network device tests: the Basic Network PCI-D3 test and the Wake-on-LAN test (described later). The basic Network PCI-D3 test verifies that, when the network device and drivers are installed in a system, the system can successfully suspend to and resume from S3.

The network device PCI-D3 test has two main steps:

1. Suspend/resume switch test (S3 state).
2. Suspend/resume staging test (S3 state).

PCI-D3 Network WOL Test

The wake-on-LAN (WOL) test makes sure that the network device supports D3 functionality. This test requires two connected systems: the target system (which has the candidate network device) and a server system (which need not be an IAPC-capable system).

The WOL test verifies that:

- When the target system is in S3 and the network device receives a WOL event from the server system (through a process automated by the PCI-D3 Network test software), the network device wakes the system properly.
- The target system's networking device is fully functional after the system resumes from S3 due to a WOL event. The server and target systems exchange a known-good file and ensure (after the system resumes from S3) that no data corruption occurs during send/receive.

PCI-D3 Audio Test

The Audio PCI-D3 test verifies that the audio hardware and drivers:

- Successfully allow the system to enter the S3 sleep state
- Successfully allow the system to wake from S3
- Are fully functional upon resume from S3

The audio functionality test consists of four main checks:

1. Suspend/resume switch test (S3 state).
2. Suspend/resume staging test (S3 state).
3. Reference application switch test (S3 state), which requires Microsoft Combat Flight Simulator.
4. Suspend/resume testing of audio devices using the DirectSound streaming test from the DirectX 7.0 SDK. This is an automated test that runs the DirectSound sample and programmatically cycles the system to the S3 state while the sample is running. The device under test passes if, on resume, no audio artifacts are noticed with the sample that is running.

Summary

Intel's PCI-D3 test suite gives you the tools to design and test graphics, audio, network, and modem peripherals in an IAPC environment. All tests must be run on a system that supports the ACPI S3 sleep state. All tests should also be run independently under Windows 98 (SE), Windows Me, and Windows 2000 (and where applicable, the upcoming Windows Whistler Operating system).

Running the PCI-D3 tests let you verify that the candidate device is D3-capable. Running the PCI-D3 tests also lets you verify that the candidate device does not degrade overall system S3 capabilities. The PCI-D3 tests are described in detail in the white paper titled *Testing Devices for D3 Compliance*, located on the Intel's Developer Update site. Motherboard developers should share these tests with their supplier hardware vendors.

Using these tools, developers can test the devices for building tomorrow's power-managed computers.

More Info

Intel's developer site includes the white paper titled, "Testing Devices for D3 Compliance." This paper describes each test and provides test specifications for graphics adapters, modems, network devices, and audio. (Note that in the white paper, the modem WOR-capability tests required a HyperTerminal application. Intel has redesigned these tests so that HyperTerminal is no longer needed.) The high-level methodology recommended for testing IAPC motherboards, devices, and systems is described in the article titled "Testing Instantly Available PCs to Ensure a Robust Product."

The IAPC Web page provides detailed information about IAPC technology and IAPC-compliant motherboards, peripherals, and drivers. Known-good motherboards, add-in cards and reference systems that can be used for IAPC-capability testing are listed in the Reference Platform Program area of Intel's developer site.

The Microsoft HCT tools and test suites are available from Microsoft. Test suites, white papers, and other information are also available in the IAPC section of Intel's developer site.

IAPC Technology Wins EPA 2000 Climate Protection Award

With its Annual Climate Protection Awards, the United States Environmental Protection Agency (EPA) honors the extraordinary accomplishments of individuals, companies, and organizations that have made significant contributions to protecting the environment. Intel's Instantly Available PC Technology was chosen along with nine others to receive this award in Washington, D.C. on October 31, 2000.

Author Bio

Ram Chary, a software systems architect in the Intel's Architecture Lab, has been with Intel 14 years. Currently, he is focusing on enabling the deployment of Instantly Available PCs. During his career, he has developed processor microcode, real-time kernels, and networking products. Ram has also managed engineering teams for multiple product releases, and has been awarded three patents. He holds a B.S.E.E. from the Indian Institute of Science, and an M.S.C.S. from the University of Minnesota.

Initiatives and Technologies

Intel Releases BIS Server Components as Open Source

Chet Johnson
Strategic Marketing Manager
Intel Architecture Lab
Intel Corporation

Overview

The ability to boot a PC to a known software configuration over the network has become widespread since the introduction of products that implement the Preboot Execution Environment (PXE). In some business environments, concerns over the security of preboot operations have delayed PXE usage, but now a standards-based solution known as Boot Integrity Services (BIS) is available. BIS plays an important role in helping safeguard PC integrity before a PC is fully operational.

As with PXE, BIS includes both a client component implemented in the system BIOS and a server component implemented in a management application. To encourage widespread support of BIS in application software, Intel is releasing the code for the BIS server component as open source. Software developers that have implemented support for PXE technology can use BIS to improve the security of a PXE network boot. BIS server components complement the BIS API (application programming interface) and services that are now becoming available on Wired for Management (WfM) enabled PCs.

The BIS server component is based on Common Data Security Architecture (CDSA) software that is also available as royalty-free open source. Unlike proprietary techniques to improve pre-boot security, BIS usage of CDSA builds upon widely accepted security-related standards including RSA or DSS digital signatures, X.509 v3 digital certificates, and Signed Manifest data integrity credentials.

Several business models of desktop PCs from IBM, Dell, and Compaq are now available with BIS as a complement to their PXE implementations. On the server side, BIS support has already been incorporated into systems management applications from Altiris, Inc., Computer Associates International, and ON Technology. Both PXE and BIS are identified in the PC 2001 System Design Guide for platforms supporting Microsoft* Whistler operating system.

Security for Remote Management

Installing new software on a PC over the network can make the PC vulnerable to unauthorized use, tampering, and accidental misconfiguration. Once exposed to such a threat, a PC's state is suspect. To help remedy this situation, a BIS API that employs public-key cryptography was defined. The BIS API enables preboot management applications to check the integrity and authorization of programs and data that are downloaded over the network. This check provides a more secure and interoperable remote boot security solution for managed PCs.

The PXE remote boot facility is the principal user of BIS to help keep client PCs safe from unauthorized access, although other software designed to run preboot may make use of these services. Initial setup of BIS and its operational usage can be characterized by the following steps:

1. *Key-pair generation*. BIS server components generate a public and private pair of cryptographic keys in the server environment. These keys identify the administrator of the client PCs that will receive downloaded programs and data and are owned by the administrator.
2. *Client configuration*. The administrator's public key is embedded into a digital certificate that is stored on each client PC.
3. *Data signing*. The administrator's private key is used to create a digital signature on the management server for each program or data file to be downloaded to a client during preboot management.
4. *Verification on download.* Whenever the management application downloads a program or data to the client during a preboot management operation, the corresponding digital signature file is also downloaded. The client program that performs the download then calls the BIS API to perform verification before allowing the data to be used or the program to be executed. BIS checks that the digital signature corresponds to the combination of the downloaded program or data as well as to the key pair for which it has the public key.

Business Benefits for Developers

The design of BIS server components is based on the CDSA (Common Data Security Architecture) specification. CDSA gives application developers access to security services by implementing a "middleware" layer between applications and security services. Instead of writing an application for a specific security service, developers write to a standard application programming interface (API). Stable, well documented APIs allow rapid adoption of emerging technologies, decrease application development cost, and reduce time-to-market by letting developers stay focused on enhancing their applications rather than building discrete security solutions.

In addition to enabling worldwide use of CDSA, BIS, and PXE technology, open source software has the advantage of lower costs, greater industry attention, and increased collaboration. CDSA, BIS, and PXE source code are publicly available for download on the Internet, free of charge from the Intel Developer Web site. Companies can view the source code to verify for themselves that no "backdoors" or security holes exist in the software.

Open source allows reuse of protocol components to ensure interoperability. Experience with open source technology such as the Linux* operating system reveals that companies can often resolve problems by examining and modifying the working code, or by collaborating with open source developers on a fix. Ultimately, the result of this open scrutiny and collaboration is software that is significantly more robust and reliable.

As a result of a recent and groundbreaking change in U.S. encryption regulations, open source security software such as CDSA and BIS can now be freely exported (except to Cuba, Iraq, Libya, Yugoslavia, North Korea, Iran, Syria, and any other country against which the U.S. has a goods embargo). This fundamental change in regulations ends the isolation between developers in different countries and allows standards-based security code to be available for use worldwide.

Open Source Manageability Technology for the EFI

To help solve certain technical BIOS boot issues, Intel has worked with several other vendors in the definition of an Extensible Firmware Interface (EFI). EFI is an OS- and platform-independent boot and preboot interface that is being implemented in new Intel® Architecture platforms including those implementing the Intel® Itanium™ processor. The EFI specification includes PXE as an existing open industry specification for enterprise network clients to automatically download software images and configuration parameters.

The EFI specification defines a new model for the interface between operating systems and platform firmware. The interface consists of data tables that contain platform-related information, plus boot and run-time service calls that are available to the operating system and its loader. Together, these provide a standard environment for booting an operating system and running preboot applications.

Summary

Intel is releasing as open source the code for the BIS server components. Initially, this software is for use on servers implementing Microsoft Windows NT* or Windows 2000 server. Before the end of the year, variations for servers running the Linux operating system and for platforms implementing EFI will be available for download. BIS server components can be deployed royalty free to enhance the security of PXE-based preboot operations without using proprietary techniques.

BIS is based on CDSA, which is being widely adapted by hardware and software vendors and is also available as open source. The release of PXE and BIS open source to the software developer community is intended to encourage developers to create more applications for the server side of PXE, and to include BIS when they do so.

More Info

For more information on BIS API, read Safeguarding the Integrity of Managed PCs.

For more information regarding CDSA, read CDSA Brings Security into the Open.

Author Bio

Chet Johnson joined Intel in 1997 and led efforts with major systems management software vendors to support the Wired for Management (WfM) initiative and WfM-enabled platforms. He currently works in Intel's Architecture Lab, with marketing responsibilities centered on networking technologies. Chet received a B.S. in electrical engineering from the University of Minnesota's Institute of Technology.

Networking and Communications

Intel® Architecture in the Voice over IP Gateway

Krishna Shetty
Applications Architect
Embedded Intel Architecture Division
Intel Corporation

Overview

The convergence of voice and data is increasing the value and usefulness of the Internet. The combination of the PSTN (Public Switched Telephone Network) and the Internet can provide access to the massive information base within the Internet through a simple mechanism like a telephone handset. Such a revolution has already begun with the introduction of standard services for voice, fax, and data that are currently delivered by the PSTN over IP- (Internet Protocol) based packet networks. The promise of transporting traditional telephony services over IP-based networks is leading to the development of cost-effective gateway equipment based on embedded systems.

Voice over IP

Voice over IP (VoIP) is essentially a way to carry voice using the IP as a transport mechanism, similar to the way data is carried in the network with TCP/IP. With the growing volume of data traffic, voice becomes yet another application over the data network.

There are currently two key applications for Voice over IP. First is the corporate network that interconnects remote branch offices with data services and would like to add voice and fax services. Corporations are interested in VoIP solutions due to the cost savings that can result through unification of two disparate networks. Apart from reducing operational and network management costs, corporations can reduce the communication access charges and settlement fees involving multi-international sites.

The second application is VoIP over various public networks. ISPs (Internet Service Providers) are increasingly interested in becoming ITSPs (Internet Telephony Service Providers), which would enable them to add voice and multimedia services and break out from the current monthly fee structure for data-only services. In addition, emerging Competitive Local Exchange Carriers (CLECs) are building new-generation IP network facilities. These carriers are interested in VoIP because it is more efficient than conventional voice networks. Finally, current POTS (Plain Old Telephone Service) providers are interested in VoIP in order to remain competitive and generate additional revenues from new services, including Local Number Portability (LNP), voice-enabled Web, unified messaging, text-to-speech conversion, etc.

In the short term, cost considerations may be the biggest motivator pushing VoIP adoption. In the long term, VoIP has potential for much more than just telephony. It promotes the convergence of services by offering flexible bandwidth for voice, fax, video, data sharing, white-boarding, and easy connectivity to various back-end services. VoIP will also promote the convergence of infrastructure by using the network bandwidth efficiently.

Building a VoIP Gateway

The evolution of IP telephony and its integration into everyday operations will require the evolution of the underlying infrastructure. Until public IP networks entirely replace the major elements of traditional telecommunication networks, the IP network and the PSTN will need to coexist.

The connectivity of dissimilar networks is achieved through the use of gateways. A gateway translates the protocols for call set-up and release, converts the media formats, and then transfers the user information between the different networks connected to it.

Equipment vendors can cost-effectively build the gateway function by embedding the VoIP technology within their legacy telecom or datacom equipment. With the massive installed base of traditional telephone equipment, gateways present a significant opportunity to telecom and datacom equipment manufacturers.

Intel® Architecture in a VoIP Gateway

As the demand for fast deployment of new services (such as VoIP services) and applications grows, fixed-function ASIC-based designs will fail to provide the needed flexibility and time-to-market advantages. Next-generation packet processing hardware will need to be both fast and easily programmable with a consistent software architecture supported by a rich assortment of hardware components offering a large spectrum of price/performance points.

Intel® Internet Exchange Architecture (IXA) is an end-to-end family of high-performance, flexible, scalable hardware and software building blocks designed to meet the growing performance requirements of today's networks. Intel® IXA solutions support faster development, cost-effective deployment, and future upgradability of network and communications systems.

Intel IXA separates the control and service functions from the wire-speed packet forwarding aspects of the communication infrastructure. This demarcation is useful in maintaining the scalability of communication systems, while allowing the individual layers to be developed independently. Such architecture can accommodate new and enhanced services and features as they emerge independent of underlying technological advances in the forwarding layer, as seen in Figure 1.

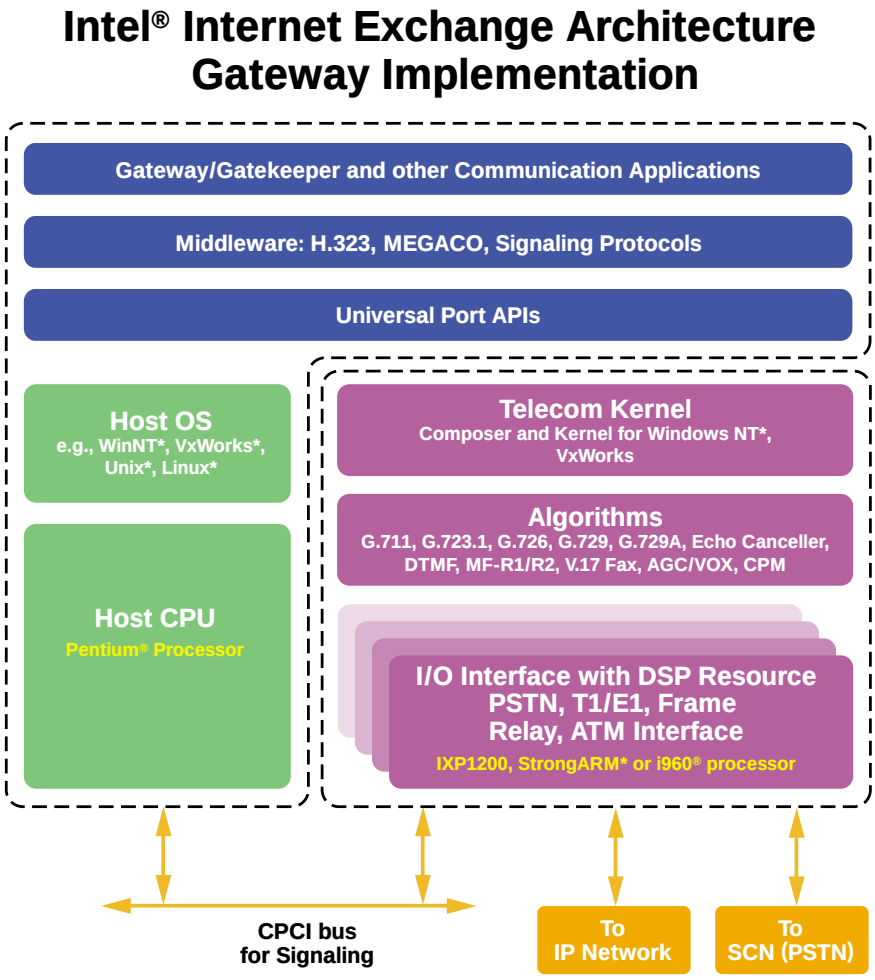


Figure 1

Embedded processors play an important role in Intel IXA by meeting processing requirements in the control and services layer. In the case of a VoIP gateway, an Embedded Intel® Architecture (EIA) processor can be used to handle the signaling stacks of both the PSTN and IP networks. In addition, EIA processors can run several other applications, including network management, supervisory, billing, and call record functions.

The I/O peripheral boards shown in Figure 1 are basically responsible for packet forwarding and other wire-speed

communication functions that are closely coupled to the physical layer. In the case of a gateway between PSTN and IP networks, the peripheral boards can handle the T1/E1 framing, ATM related functions, or other higher-speed PSTN interfaces. These I/O boards also provide the interface to the IP network and media related algorithms, RTP/RTCP protocols, and packetization. Depending on the port density, speed, and complexity of I/O functions, these boards can utilize the network processor or Intel® i960® processors.

ACPP and Software Vendors

Time-to-market is a key factor in the development of communications equipment, particularly products dealing with the Internet infrastructure. With this view in mind, the Intel® Applied Computing Platform Providers (ACPP) program has been established and supports the development of embedded Intel Architecture platforms for communications applications. In addition, Intel is working with software vendors to port, optimize and validate new signaling, media control, and management stacks on Intel® processors.

Summary

A carrier-class VoIP gateway can be built around Intel Internet Exchange Architecture (IXA) by optimally partitioning the control and signaling layers and the media protocol layers between the host CPU and the I/O processors. Intel provides a comprehensive range of processors and associated chipsets for both the host and I/O peripheral boards. In addition, Intel has launched key programs with platform and software vendors to accelerate the development of communication platforms and gateways that enable new and enhanced services for the Internet.

More Info

To read the full white paper on Voice over IP, visit the newly redesigned Embedded Intel Architecture in Communications Web site.

For more information on Intel Internet Exchange Architecture solutions, visit the IXA Web site.

For more information on the Intel Applied Computing Platform Provider (ACCP) Program, visit the ACPP Web site.

Author Bio

Krishna Shetty is an applications architect in the Communications group in the Embedded Intel Architecture Division. He has worked for Intel for five years. Prior to joining Intel, Krishna worked in defining and developing integrated circuits for voice and data communications. Earlier in his career, he designed and developed telemetry and command systems for satellites and satellite launch vehicles in India. Krishna has a degree in telecommunications from Karnatak University in India.

Software

Intel® XML-based Solutions for e-Business Data Centers

Jay Jeyaseelan
Sr. Technical Marketing Engineer
Communications Products Group
Intel Corporation

Overview

The growing need to complete business-to-business (B2B) and business-to-consumer (B2C) transactions securely and reliably via the Internet requires systems talking to systems–systems with diverse networks and databases. Until recently, Electronic Data Interchange (EDI) was a common method used for the transfer of data among different companies. With the growing popularity of e-Commerce, EDI became an increasingly important mechanism for companies to use in buying, selling, and trading information. However, the cost of dedicated proprietary EDI servers, software, IT resources, Value Added Network overhead charges, and the steep learning curve with the EDI format can overwhelm many companies. Many small or medium-size companies that want to implement online business systems are finding it difficult due to the high initial EDI infrastructure costs.

Today, eXtensible Markup Language (XML) is emerging as the cross-platform data format standard for e-Business. Rapidly eclipsing EDI as a universal data exchange tool, XML tags data with precise, customized descriptions for various servers, applications, users, and devices. It may be integrated easily with existing Web infrastructure and other e-Business programming languages.

XML also offers a cost-effective alternative to EDI for most companies. It takes full advantage of the Internet as a means to conduct B2B transactions 24 by 7. Therefore, businesses need only PCs, servers, and the existing network infrastructure to implement online business transaction systems. As this markup language deals with text and structure of text data, it is easy to learn, program, and implement.

New Standards for e-Business Transactions

Major industry players are adopting XML as the standard for e-Business transactions because of its technical and business advantages. In an article titled “Major Retailers Back XML” published in the August 4 issue of *InfoWorld.com*, writer Eugene Gryco reports the Global Commerce Initiative (GCI) recently adopted XML-based standards recommended by the Organization for the Advancement of Structured Information Standard (OASIS), and the U.N. Center for the Facilitation of Procedures and Practices for Administration, Commerce and Transport (UN/CEFACT). These organizations developed the technical infrastructure standards, which cover data access and security, basic data content, and basic information flow.

Developing XML-based e-Business Applications

Stemming from SGML as well as HTML, and designed especially for Web documents, XML allows developers to create their own customized tags, enabling the definition, transmission, validation, and interpretation of data between applications and between organizations.

Developers are now creating XML-based applications, and Intel is helping to drive XML adoption with a family of XML networking appliances. These scalable, drop-in appliances enhance XML applications by addressing several key e-Business challenges–slow response time, dropped connections and dead servers, and incompatible protocols and languages.

Business Rule-Based Traffic Management

The patent-pending rules-based XML engine is an intelligent application that resides on the Intel® NetStructure™ XML Accelerator appliance. The XML engine uses programmable business rules to classify each e-Business transaction, then directs the transaction traffic to the appropriate application server. The engine works with several XML dialects based on the industry-standard XML 1.0, such as Microsoft* BizTalk* Framework, CommerceOne* Common Business library (xCBL), Ariba* implementations of the Commerce XML open standard (cXML), and other open standard dialects such as Electronic Business XML (ebXML).

The Intel NetStructure 7210 XML Accelerator, which was awarded Grand Prize Best of Show at the May 2000 Networld+Interop, improves XML transactions by accelerating and offloading secure XML–up to 600 SSL connections per second while classifying key XML transactions.

The Intel NetStructure 7280 XML Director not only accelerates secure XML traffic–up to 1,200 SSL connections per second–but also intelligently directs XML e-Business traffic based on programmable, user-specified business rules.

Acceleration and Navigation Advantages

The Intel NetStructure XML Accelerator family of products provide Secure Socket Layer (SSL) acceleration, offloading this processor-intensive task from the Web servers. Therefore, Web server investments are maximized and server bottlenecks are reduced.

The patent-pending XML engine is based on XPath 1.0, the industry-standard XML path language. XPath directs the software through the document. When navigating through an XML document, a path is created from one point to another. The navigation language is needed to describe a way to move about a document, to describe a section of a document that needs to be transformed, and to be able to point to a certain part of the document. Intel's implementation of XPath models an XML document as a tree of nodes of the following types: element, attribute, and text.

Parsing

The Intel NetStructure XML Accelerator family of products also utilize a parsing program for processing XML documents. This program breaks down the textual representation of a document and turns it into a set of conceptual objects. The program can also perform a "well-formness" check of the XML code before directing the transaction to the XML application server to reduce the risk of errors.

Summary

XML is considered the HTML of business systems. It is replacing many specialized and proprietary formats for e-Business transactions, such as EDI. A standard, universal data interchange tool, XML provides a system for defining specialized markup languages used to transmit data. It is emerging as the new foundation of B2B and B2C, allowing for the integration of trading partners, services, and business processes.

Developers for companies that engage in e-Business are creating applications and supporting tools that take advantage of XML benefits. The Intel NetStructure XML Accelerator family of products allow developers to create XML-based applications that offer greater management and performance for key XML transactions.

More Info

You can find more information on XML and the family of Intel NetStructure XML Accelerators at the following Web sites.

- Intel NetStructure XML Accelerators
- XML for B2B E-Commerce Solutions
- WC3 Architecture Domain
- XML Org
- The XML Files
- What is XML?
- XMLInfo
- EBXML–OASIS Site
- OASIS–The XML Cover Pages

Author Bio

Jay Jeyaseelan provides technical marketing support for the Intel NetStructure XML Accelerator product line. Before joining the Network Equipment Division in June, Jay held technical lead, sustaining engineering manager, and project manager roles in Intel e-Business Content Delivery System Projects. He has received divisional recognition awards for his work on the Intel Secret–Information Desk project, a Web-based application that allows Intel customers to receive Intel® Secret (yellow cover) documents electronically. He has also received team recognition awards for his contributions to the Intel Field Division Business Link project. Jay has an M.S. in mechanical engineering from the University of Maryland, an M.S. in materials science from North Carolina A&T State University, and a B.S. in civil engineering from Madurai University in Madurai, India.

—End of Intel Developer Update Magazine Issue 15—